Record-Low Metal to Semiconductor Contact Resistance in Atomic-Layer-Deposited In_2O_3 TFTs Reaching the Quantum Limit

C. Niu[1,†], Z. Lin[1,†], Z. Zhang[1], P. Tan[1], M. Si[1], Z. Shang[2], Y. Zhang[2], H. Wang[2] and P. D. Ye[1,*]
[1]Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA,
[2]School of Materials Engineering, Purdue University, West Lafayette, IN, USA
[†]These authors contributed equally to this work, *Email: yep@purdue.edu

***Abstract*—** In this work, we demonstrate the record-low metal-to-semiconductor contact resistance $R_c = 23.4\ \Omega\ \mu m$ at $n_{2D} = 5.0 \times 10^{13}\ cm^{-2}$ (reaching the quantum limit) in atomic-layer-deposited (ALD) In_2O_3 thin-film transistors (TFTs) with back-end-of-line (BEOL) compatibility. Our long-channel devices ($L_{ch} = 1\ \mu m$) exhibit excellent drain current saturation, while our short-channel devices ($L_{ch} = 50\ nm$) achieve high on-current performance ($2.6\ mA/\mu m$ at $295\ K$, and $5.4\ mA/\mu m$ at $10\ K$). The superior ohmic contact is made possible by the charge neutrality level (CNL) deeply aligned inside the conduction band of In_2O_3, which can also be understood as an interfacial donor-like trap-induced negative Schottky barrier. Notably, we investigate the contact resistance at various temperatures, O_2 annealing conditions, and channel thicknesses, providing a comprehensive understanding of this material system. Furthermore, we demonstrate an ultra-low contact resistivity of $\rho_c \approx 1.3 \times 10^{-9}\ \Omega\ cm^2$ and current transfer length of $L_T \approx 2\ nm$ in $1\ nm$ thin films. These findings position In_2O_3 as a highly promising candidate for ultra-scaled, high-performance BEOL transistors from the contact engineering point of view.

I. Introduction

As the Si CMOS technology has scaled to 3 nm node and beyond, the importance of contact resistance has increased due to the decreasing channel resistance. In the near ballistic region, the total on-resistance of a transistor is primarily determined by the contact. Minimizing the contact resistance is crucial for the industry to further downscale CMOS and extend Moore's law. The contact resistance between metal and semiconductor originates from the thermal injection of electrons over the Schottky barrier, which is mostly dominated by the so-called Fermi-level pinning. The contact resistance is also influenced by the number of modes inside of the semiconductor channel (quantum limit). Engineering the contact can lead to the improved device performance.

Recently, there has been significant interest in BEOL device technology for monolithic 3D integration. Amorphous oxide semiconductors are considered promising candidates for BEOL channel materials due to their low thermal budget requirements and compatibility with large wafer-scale fabrication. ALD In_2O_3 TFTs have shown great potential, offering high uniformity and conformability in large wafer-scale production, controllable channel thickness, and excellent performance with a mobility exceeding 100 $cm^2/V{\cdot}s$ [1], on-current approaching 20 mA/μm [2], and ultra-high bias stability [3].

In this report, we present ALD In_2O_3 TFTs exhibiting ultra-low contact resistance and high on-current of 5.4 mA/μm, achieved through the realization of a negative Schottky barrier. The device's behavior is studied over a temperature range of 10 K to 295 K, and the CNL is found to be crucial in understanding the contact resistance. Reducing the contact resistance of the transistor further enables shorter delays in logic applications. Our work provides a new insight for how to engineer and significantly improve contacts in future transistors with aggressively scaled atomically thin channels.

II. Experiments

The device structure of a bottom gate In_2O_3 FET is illustrated in Fig. 1. Fig. 2 shows the fabrication process flow. As the bottom gate metal, 40 nm Ni was deposited onto 90 nm SiO_2/Si substrate by e-beam evaporation. 3 or 5 nm HfO_2 gate dielectric was grown by ALD at 200 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf) and H_2O as Hf and O precursors. 1-3 nm channel In_2O_3 were then deposited by ALD at 225 °C, using $(CH_3)_3In$ (TMIn) and H_2O as In and O precursors. The film thickness is accurately controlled by the ALD cycles. Channel isolation was done by wet etching of In_2O_3 using concentrated hydrochloric acid, followed by the deposition of 80 nm Ni as source/drain contacts. O_2 annealing at various temperatures (190 to 400 °C) is optional. Note that the whole process is BEOL compatible with a low thermal budget of 400 °C even considering high temperature O_2 annealing. Fig. 3 and 4 show the top and cross-section view of a fabricated In_2O_3 FET with L_{ch} of 50 nm using a scanning electron microscope (SEM) and transmission electron microscopy (TEM), respectively. The energy dispersive x-ray spectroscopy (EDS) mappings confirm the presents of ALD In_2O_3 and HfO_2.

The electrical characterization at room temperature (295 K) was measured with the Keysight B1500 system in a Cascade probe station. The temperature-dependent characterization (10 K to 295 K) was performed in a Lakeshore CRX-VF cryogenic probe station. The threshold voltages are determined by the linear extrapolation method based on the transfer characteristics. More than 100 devices were measured.

III. Results and Discussion

The typical transfer and output characteristics of a long channel In_2O_3 FET with L_{ch} of 1 μm at 295 K and 10 K are presented in Figs. 5 and 6, with current saturation at a large V_{DS}. Higher V_{DS} can be applied due to the low self-heating effects (SHE) under low temperatures. The on-current is slightly decreased at low temperature at the same V_{DS} and V_{GS} because the threshold voltage V_T shifted +1.5 V due to the carrier freezing when the temperature is cooled down to 10 K. Figs. 7 and 8 show the typical transfer and output characteristics of a short channel In_2O_3 FET with L_{ch} of 50 nm at 295 K and 10 K with high on-current (2.6 mA/μm at 295 K,

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and 5.4 mA/μm at 10 K) attributed to the high electron velocity of ALD In_2O_3. [4] Note that the on-current is increasing at low temperatures at the same V_{DS} and V_{GS} while the V_T is shifted +1 V. This can be explained by the negative Schottky contact-induced extra charge, which will be discussed in the following section, and the In_2O_3 mobility increase.

Fig. 9 illustrates the trap density at the In_2O_3 interface. The CNL and the Fermi level are deeply inside the conduction band. As a result, the interface charge is donor-like (neutral when full and positively charged when empty) mainly due to the Oxygen vacancies. The band alignment of metal and semiconducting In_2O_3 junction is shown in Fig. 10. The positive interfacial trap charges Q_{ss} induces negative space charges Q_{sc} inside the In_2O_3 channel according to the charge balance, resulting in a negative Schottky contact barrier and the channel accumulation, in great contrast to conventional semiconductors such as Si and III-V, whose interfaces have positive Schottky barriers and depletion regions.

The temperature-dependent transfer characteristics of an In_2O_3 FET with L_{ch} of 1 μm were measured from 295 to 33 K, as shown in Fig. 11. The dashed line indicates the gate-leakage current. The V_T gradually shifted positively when the temperature decreased. The Arrhenius plot is shown in Fig. 12 by plotting the $ln(I_D/T^{1.5})$ vs. $1000/T$ using the data from Fig.11. The V_{GS}-dependent effective Schottky barrier height Φ_B is then calculated from the slopes in Fig.12 and summarized in Fig. 13. The Schottky barrier height Φ_{SB} is negative at the flat band condition. The positive Φ_B measured at small V_{GS} originates from the energy difference between the In_2O_3 under metal contact and the In_2O_3 channel depleted by the gate voltage, not the metal-to-semiconductor contact. The Φ_B is also calculated in a short channel device with L_{ch} of 40 nm. The negative contact barrier height is observed at all gate biases, indicating that the trap at the metal-semiconductor interface affects the channel band alignment, which is in agreement with the previous transfer and output curves in short channel devices. It is worth mentioning that the thermionic emission model is no longer valid if the barrier height is negative. The deviation from the linear dispersion at low temperatures ($T < 175\ K$) and the positive slope at high gate biases in the Arrhenius plot provide strong evidence that the contact barrier height is negative.

Because of the negative Schottky barrier height, the contacts maintain ohmic behavior at 10 K. Fig. 14 shows an excellent linear relation between I_D and V_{DS} at various V_{GS}-V_T. The L_{ch}-dependent transfer characteristics are plotted in Fig. 15. The carrier density n_{2D} dependence of the contact resistance R_c can be extracted by the transfer length method (TLM) by fitting the total resistance vs. L_{ch}, as shown in Fig. 16. The intercept and the slope of the linear fitting are $2R_c$ and sheet resistance R_{sh}, respectively. Good linearity ensures the accurate extraction. The carrier density is estimated using $n_{2D} = C_{ox}(V_{GS} - V_T)/q$, where $C_{ox} = 1.6 \times 10^{-6}\ F/cm^2$ for 5 nm HfO_2. According to the Landauer–Büttiker formula, the contact resistance is limited by the number of modes inside the semiconductor ($M = Wk_F/\pi$, where k_F is the Fermi vector, W is the width), where each mode contributes a conductance of $G_0 = 2e^2/h$. Fig. 17 shows the extracted R_c and the calculated quantum limit. In single crystals, $k_F = \sqrt{2\pi n_{2D}}$ without valley degeneracy. In amorphous In_2O_3, the Fermi vector is larger at the same carrier density due to the disorder-induced localized states, resulting in a smaller R_c. Furthermore, the negative-Schottky-barrier-induced In_2O_3 accumulation under the contact could also lead to the underestimation of carrier density. These facts might lead the experimental R_c below the quantum limit. A low contact resistivity of $\rho_c \approx 2 \times 10^{-9}\ \Omega\ cm^2$ is obtained with weak dependent on the n_{2D} in Fig. 18. Fig. 19 shows that R_c is weakly dependent on the temperature at different carrier densities, indicating that R_c is reaching the quantum limit.

Figs. 20-22 shows the effect of O_2 annealing on the device and the contact resistance. The oxygen vacancies (donor-like trap) were filled after annealing, resulting in a lower CNL. The V_T shifted positively. The R_c increases after higher temperature annealing due to the less negative barrier height. Figs. 23-25 shows the effect of channel thickness T_{ch} on the device and the contact resistance. The V_T shifted positively and the sheet resistance (extracted using TLM) increased when T_{ch} is reduced. An extremally small contact resistivity of $\rho_c \approx 1.3 \times 10^{-9}\ \Omega\ cm^2$ and current transfer length of $L_T \approx 2\ nm$ are achieved in the 1 nm thick In_2O_3 TFTs, establishing an excellent foundation for the development of ultra-scaled device technology. Fig. 26 shows the benchmark of the contact resistance R_c as a function of carrier density n_{2D} of In_2O_3 TFTs with other semiconductors [5-15] including: Si, III-V, MoS_2, and amorphous oxides. This work demonstrates the achievement of the smallest contact resistance, pushing it to the quantum limit.

IV. Conclusion

In conclusion, this study demonstrates the impressive performance of ALD In_2O_3 TFTs at both room temperature (295 K) and low temperature (10 K). The presence of negative Schottky barriers, facilitated by CNL alignment, is observed. The achievement of excellent ohmic contact with record-low contact resistance (R_c) reaching the quantum limit is a significant breakthrough for contact engineering on novel channel materials. Notably, ultra-low contact resistivity and current transfer length are achieved in In_2O_3 TFTs with a 1 nm channel thickness. These findings provide strong foundation for considering ALD In_2O_3 as a promising BEOL oxide semiconductor channel material for next-generation high-performance BEOL electronics.

Acknowledgment

The work is supported by AFOSR, SRC nCore IMPACT Center and DARPA/SRC JUMP ASCENT Center.

References

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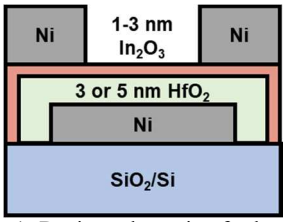

Fig. 1. Device schematic of a bottom gate In_2O_3 FET.

- ❑ SiO_2/Si substrate cleaning
- ❑ Bottom gate deposition: e-beam evaporation; 40 nm; Ni
- ❑ Gate dielectric deposition: ALD; 3 or 5 nm; HfO_2
- ❑ Channel deposition: ALD; 1-3 nm; In_2O_3
- ❑ Isolation: wet etching; concentrated hydrochloric acid
- ❑ Source/Drain deposition: e-beam evaporation; 80 nm; Ni
- ❑ O_2 annealing (optional)

Fig. 2. Fabrication process flow of In_2O_3 FETs.

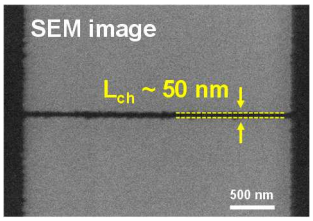

Fig. 3. SEM image of an In_2O_3 FET with the L_{ch} of 50 nm.

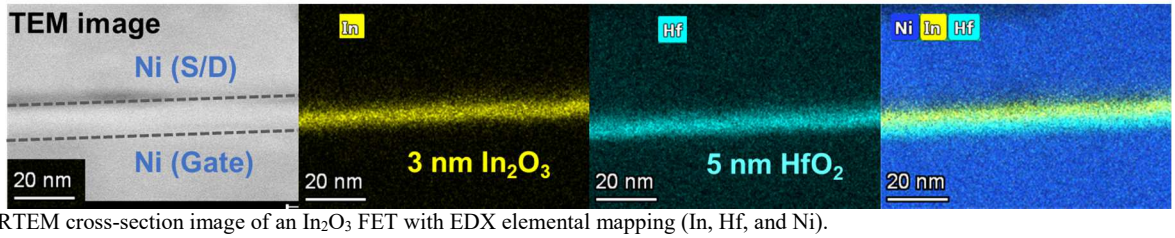

Fig. 4. HRTEM cross-section image of an In_2O_3 FET with EDX elemental mapping (In, Hf, and Ni).

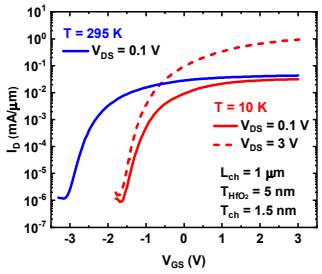

Fig. 5. Transfer characteristics of an In_2O_3 FET with the L_{ch} of 1 μm at 295 K (blue) and 10 K (red).

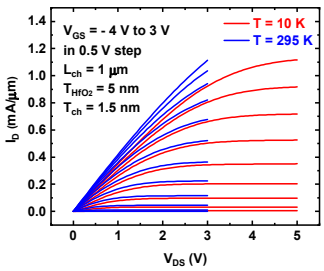

Fig. 6. Output characteristics of an In_2O_3 FET with the L_{ch} of 1 μm at 295 K (blue) and 10 K (red), showing saturation at large V_{DS}.

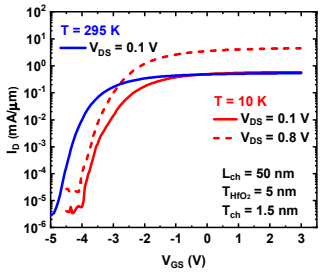

Fig. 7. Transfer characteristics of an In_2O_3 FET with the L_{ch} of 50 nm at 295 K (blue) and 10 K (red).

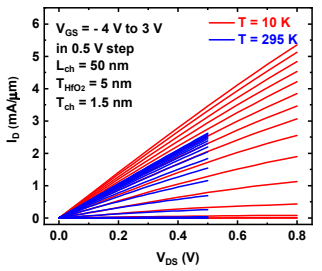

Fig. 8. Output characteristics of an In_2O_3 FET with the L_{ch} of 50 nm at 295 K (blue) and 10 K (red). The on-current is larger at 10 K.

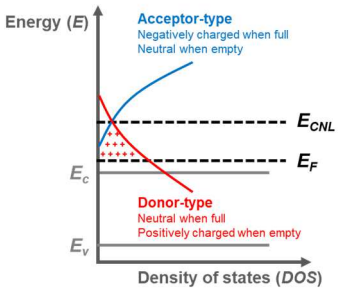

Fig. 9. Schematic of the trap density at the In_2O_3 interface. The Fermi level E_F is above the conduction band edge E_c. The charge neutrality level E_{CNL} is located deeply inside the conduction band.

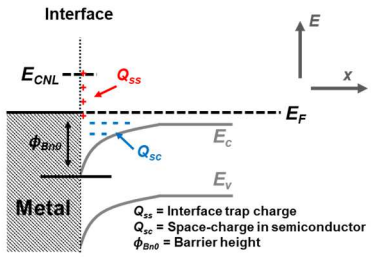

Fig. 10. Schematic of the semiconductor (In_2O_3) and metal (Ni) junction band alignment. The positive charges at the interface further bend the conduction band of In_2O_3, resulting in a negative Schottky barrier.

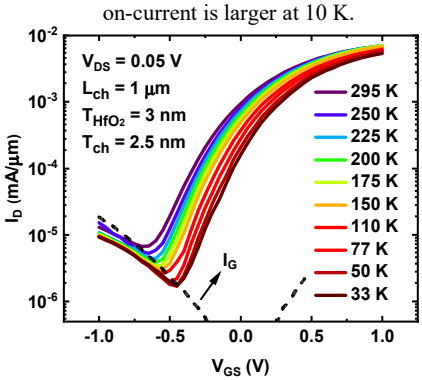

Fig. 11. Temperature-dependent transfer characteristics of an In_2O_3 FET. Gate leakage current is shown in a dashed line.

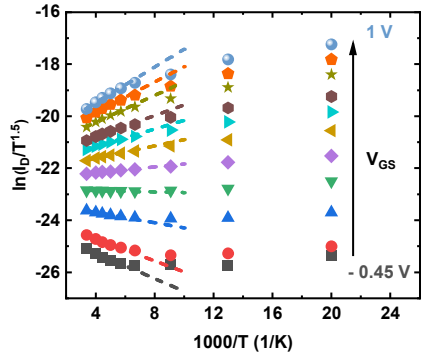

Fig. 12. The Arrhenius plot at different gate biases extracted from Fig.11. The data is linearly fitted at high temperatures ($T \geq 175\ K$).

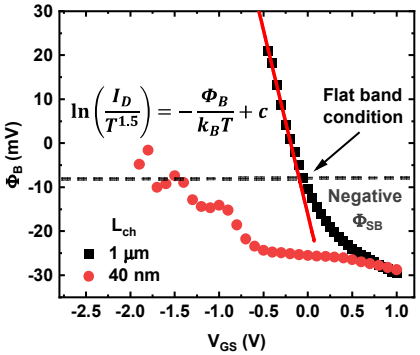

Fig. 13. The extracted contact barrier height Φ_B at various gate biases, showing a negative Schottky barrier. The positive contact barrier height in the 1 μm device originated from the gate-induced channel depletion inside In_2O_3.

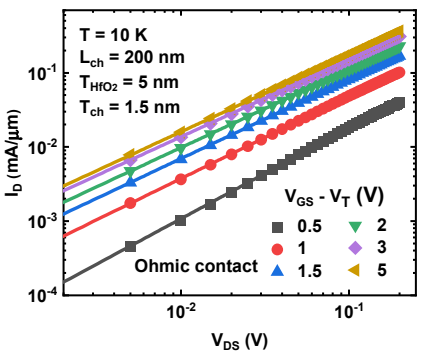

Fig. 14. The logarithmic plot of the I_D-V_{DS} curve at different V_{GS}-V_T. The linear fitting shows excellent ohmic contact at 10 K.

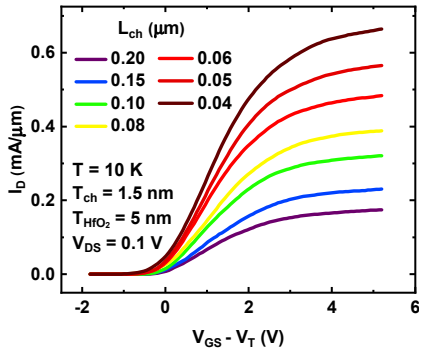

Fig. 15. Channel length L_{ch} dependence of the transfer curves at 10 K.

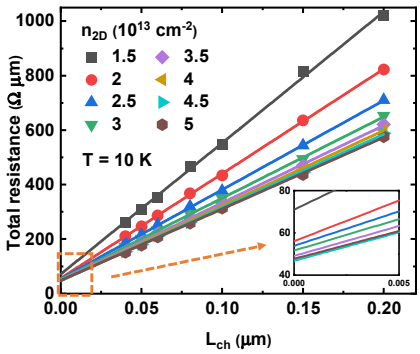

Fig. 16. Contact resistance R_c extraction at different carrier densities by TLM method. Inset: magnified plot showing the intercepts.

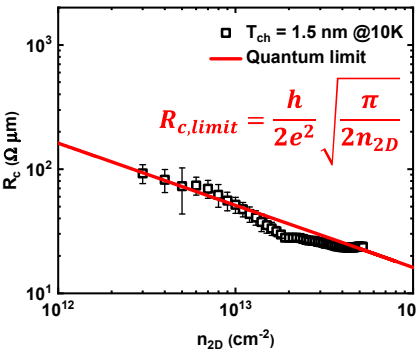

Fig. 17. Carrier density dependence of the contact resistance R_c. The red line is the theoretically calculated quantum limit of the contact resistance.

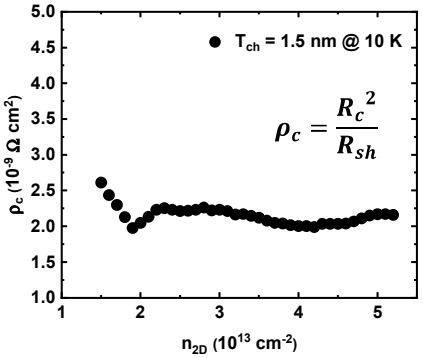

Fig. 18. Contact resistivity ρ_c as a function of the carrier density.

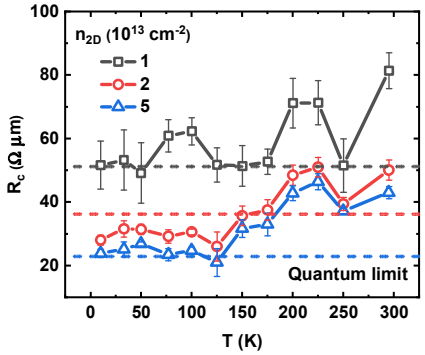

Fig. 19. Temperature dependence of the contact resistance R_c at different carrier densities.

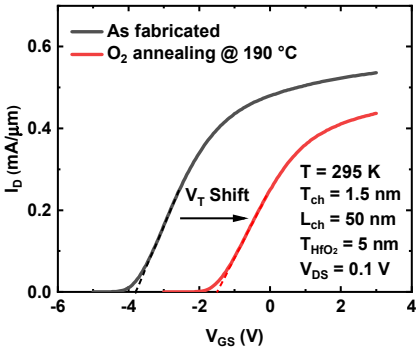

Fig. 20. Transfer characteristics of an In_2O_3 FET after O_2 annealing. The threshold voltage V_T shifts positively.

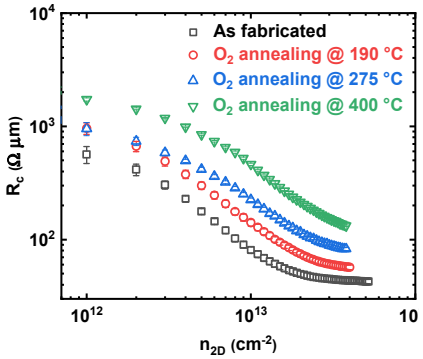

Fig. 21. Carrier density dependence of the contact resistance R_c at different O_2 annealing temperatures.

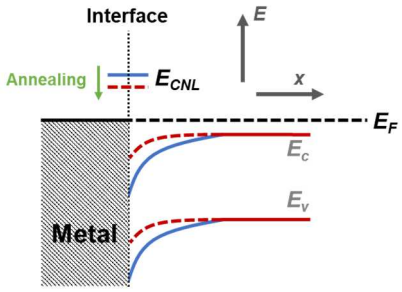

Fig. 22. Model of contact band alignment after O_2 annealing. The decrease of positive charges at the interface lowers the carrier density of the In_2O_3.

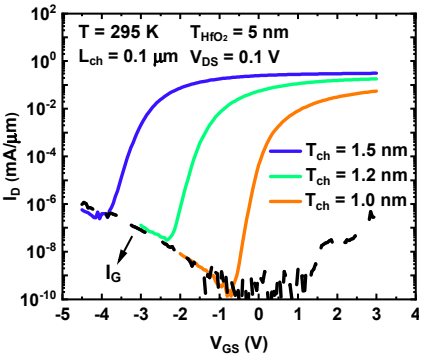

Fig. 23. Transfer characteristics of In_2O_3 FETs with different channel thickness T_{ch}. Gate leakage current is shown in a dashed line.

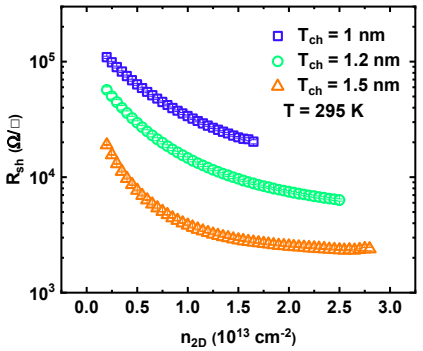

Fig. 24. Carrier-density-dependent sheet resistance R_{sh} at various channel thicknesses extracted from the TLM method.

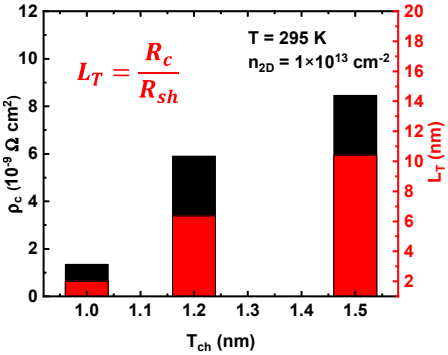

Fig. 25. Channel thickness dependence of the contact resistivity ρ_c and current transfer length L_T. The extremely small L_T is preferred for contact length scaling in ultra-scaled devices.

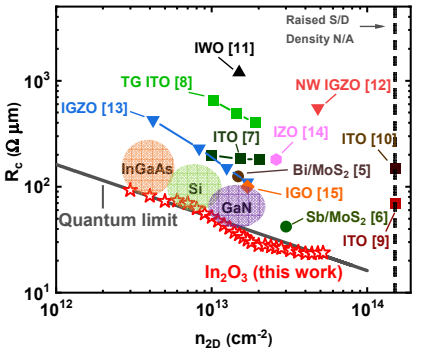

Fig. 26. Benchmark of R_c as a function of carrier density n_{2D} for semiconductors including III-V, Si, MoS_2, and amorphous oxides. This work shows the smallest contact resistance reaching the quantum limit.